WHAT IS CLAIMED IS:

1. Structure comprising:

a substrate formed of a heat deformable material;

at least one semiconductor die embedded in said substrate such that the top surface(s) of said at least one semiconductor die and the top surface of said substrate are in substantially the same plane;

a plurality of bonding pads formed on the top surface(s) of said at least one die; and

a plurality of conductive paths formed over the top surface(s)of said at least one die and the top surface of said substrate, each conductive path ending on the top surface of said substrate in a conductive land or pad and beginning in electrical contact with a corresponding bonding pad on said at least one die thereby to connect said corresponding bonding pad on the top surface(s) of said at least one die with a corresponding conductive land or pad on the top surface of said substrate.

2. Structure as in Claim 1 including a plurality of conductive balls, each ball being formed on a corresponding one of the conductive lands or pads on the top surface of said substrate, said conductive balls allowing said structure to be electrically connected to electrical contacts on an additional substrate.

3. Structure as in Claim 2 wherein said additional substrate is a printed circuit board.

4. Structure as in Claim 3 wherein said printed circuit board includes electrically conductive traces connected to said electrical contacts thereby to allow electrical signals to be sent from said at least one die to circuitry external to said at least one die and to also allow electrical signals to be sent from circuitry external to said at least one die to said at least one die.

5. Structure as in Claim 1 wherein the top surface(s) of said at least one die is (are) protected by a protective coating thereby to prevent contaminants or moisture from

reaching the top surface(s) of said at least one die and to act as a barrier between the semiconductor material and the conductive paths.

6. Structure as in Claim 5 wherein said protective coating is selected from the group of materials consisting of plastic, polyimide and other photosensitive polymers.

7. Structure as in Claim 5 wherein said protective coating covers the top surface(s) not only of said at least one die but also of said substrate.

8. Structure as in Claim 1 including

a second set of bonding pads on a bottom surface of said substrate opposite to the top surface of said substrate; and

a set of conductive vias in said substrate, each conductive via connecting one of the bonding pads on the bottom surface of said substrate to a corresponding bonding pad on the top surface of said substrate.

9. The method of fabricating a package for at least one semiconductor die which comprises:

forming a substrate of a material deformable at a temperature elevated relative to room temperature;

heating said substrate until the substrate material is deformable;

pressing at least one semiconductor die into said substrate until the top surface of said at least one semiconductor die occupies a selected position relative to the top surface of said substrate; and

cooling said substrate thereby to embed said integrated circuit die in said substrate material.

10. The method of Claim 9 wherein the step of cooling said substrate comprises allowing said substrate to cool in a room temperature or specifically controlled temperature environment.

11. The method of Claim 9 including the step of forming at least one conductive path on the top surface(s) of said at least one semiconductor die and substrate, said at least one conductive path terminating in a conductive land on the top surface of said substrate thereby to interconnect a bonding pad on the top surface(s) of said at least one semiconductor die to said conductive land.

12. The method of Claim 9 wherein the at least one semiconductor die is pressed into said deformable substrate material until the top surface(s) of said at least one semiconductor die is (are) substantially coplanar with the top surface of said substrate.

13. The method of Claim 11 wherein the step of forming said at least one conductive path and conductive land connected to a bonding pad on the top surface of said at least one semiconductor die comprises:

forming a layer of conductive material on the top surface(s) of said at least one semiconductor die and said substrate; and

forming said layer of conductive material into said at least one conductive path and said conductive land connected to one end of said conductive path.

14. The method of Claim 13 wherein forming said layer of conductive material into said at least one conductive path comprises forming said layer of conductive material into a plurality of conductive paths and lands, each path terminating on top of said substrate as a conductive land.

15. The method of Claim 9:

wherein the at least one semiconductor die contains a plurality of bonding pads on said top surface(s) of said at least one semiconductor die; and

wherein each conductive path between one of said bonding pads on the top surface(s) of said at least one semiconductor die terminates in a conductive land on the top surface of said substrate.

16. The method of Claim 13 wherein each of the conductive paths terminating in a conductive land is formed by

providing a conductive layer on the top surface of the structure; and

patterning said conductive layer into a plurality of conductive paths and conductive lands using photolithographic techniques.

17. The method of Claim 13 including:

forming at least one conductive land on a bottom surface of said substrate opposite said top surface; and

forming at least one conductive via from the at least one conductive land on the bottom surface of said substrate to the at least one conductive land on the top surface of said substrate.

18. Structure as in Claim 1, including:

at least one conductive plane formed over at least a portion of at least one top surface of said at least one die, said conductive plane being electrically insulated from selected ones of said plurality of bonding pads formed on the top surface of said at least one die.

19. Structure as in Claim 18 wherein said conductive plane is formed in a region interior to said plurality of bonding pads on at least one top surface of said at least one die.

20. Structure as in Claim 19 wherein said conductive plane is connected to one or more selected electrical contacts so as to be capable of providing a voltage from the group of voltages consisting of ground and Vcc.

21. Structure as in Claim 19 wherein said conductive plane has at least one connection to at least one of the bonding pads formed on the at least one top surface of said at least one die thereby to allow a selected potential to be applied to said conductive plane.

22. Structure as in Claim 18 wherein:

said at least one conductive plane has formed over the top surface thereof a protective coating of an insulating material;

at least one opening is formed through said protective coating of insulating material to expose a portion of the top surface of said conductive plane; and

a conductive material is placed in said opening to allow both electrical connection to be made to said conductive plane and to allow heat to be transferred from said conductive plane.

23. Structure as in Claim 22 wherein:

said protective coating has a plurality of openings formed in the top surface thereof and a plurality of conductive materials formed in said corresponding plurality of openings, each conductive material in a selected opening being capable of providing electrical connection to said conductive plane and allowing heat to be transferred from said conductive plane to an external sink or substrate.

24. Structure as in Claim 23 wherein:

said conductive material comprises lead balls formed in each of said openings in said protective coating, said lead balls being capable of being connected to a printed circuit board, thereby to allow electrical potential to be applied to said conductive plane and heat to be transferred from said conductive plane.

25. Structure as in Claim 18, including:

a bottom electrically conductive plane formed on the surface of said substrate opposite said top surface.

26. Structure as in Claim 25, including:

at least one electrically conductive connection formed to connect said bottom electrically conductive plane to a source of electrical potential.

27. Structure as in Claim 26 wherein said source of electrical potential is selected from a group of voltage sources capable of providing ground and Vcc.

28. Structure comprising:

a substrate formed of a heat deformable materials;

a semiconductor die embedded in said substrate such that the top surface of said semiconductor die and the top surface of said substrate are both exposed;

a plurality of bonding pads formed on the top surface of said semiconductor die; and

a plurality of conductive paths formed over the top surface of said semiconductor die and over the top surface of said substrate, each conductive path ending on said top surface of said substrate as a conductive land, and beginning on said semiconductor die in electrical contact with one of said plurality of bonding pads.

29. Structure as in claim 20 wherein:

the top surface of said semiconductor die and the top surface of said substrate are substantially coplanar.